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Features

- Supports fast graphics operations with bitmaps
- 2.5D option – enables perspective correct texture rendering in 3D
- Solid fill – rectangle rendering with any color
- Solid fill – triangle rendering with any color
- Triangle rendering with texturing: used for bitmap rotation, transformation or scaling
- Supports two different filtering methods:
 - point sampling (the nearest neighbor interpolation)
 - bilinear interpolation
- Texture swizzling storage option – for the highest speed texture rendering
- Clamp to edge texture rendering
- Supports 32bpp (True Color 24-bit with alpha channel) bitmap pixel memory layout
- Configurable registers interface compliant to the CoreConnect™ OPB or PLBv46 bus specifications
- Works with configurable (32 or 64 bits) Xylon logiMEM and Xilinx MPMC memory controllers.
- Other memory bus interfaces can be supported on request

Core Facts	
Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design ucf
Verification	Reference design simulation
Reference Designs & Application Notes	XPS reference design
Additional Items	logiCRAFT6 evaluation board logiTAP evaluation platform SW drivers
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LCs	Slices ¹ (FFs/ LUTs)	IOB	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
	mclk	rcclk									
Spartan®-3 (XC3S400-5)	80	160	7797	3465	0	0	4	12	0	N/A	ISE® 12.4
Spartan®-3adsp (XC3SD1800A-5)	100	160	7689	3417	0	0	3	12	0	N/A	ISE® 12.4
Spartan®-6 (XC6SLX45T-3)	160	133,33	8692	1358	0	0	3	12	0	N/A	ISE® 12.4
Virtex®-4 (XC4VLX40-12)	160	266	7853	3490	0	0	3	12	0	N/A	ISE® 12.4
Virtex®-6 (XC6VLX75T-3)	200	266	7968	1245	0	0	3	12	0	N/A	ISE® 12.4

Notes:

- 1) Configuration with 32-bit XMB memory interface, Slave PLB register interface, 64 words burst size, texture cache depth of 4 kB, texture cache line size of 8 pixels, and video stride width set to 1024 pixels. Source and destination bitmap coordinates width both set to 1024 pixels. Solid fill option turned on and 2.5D mode disabled.

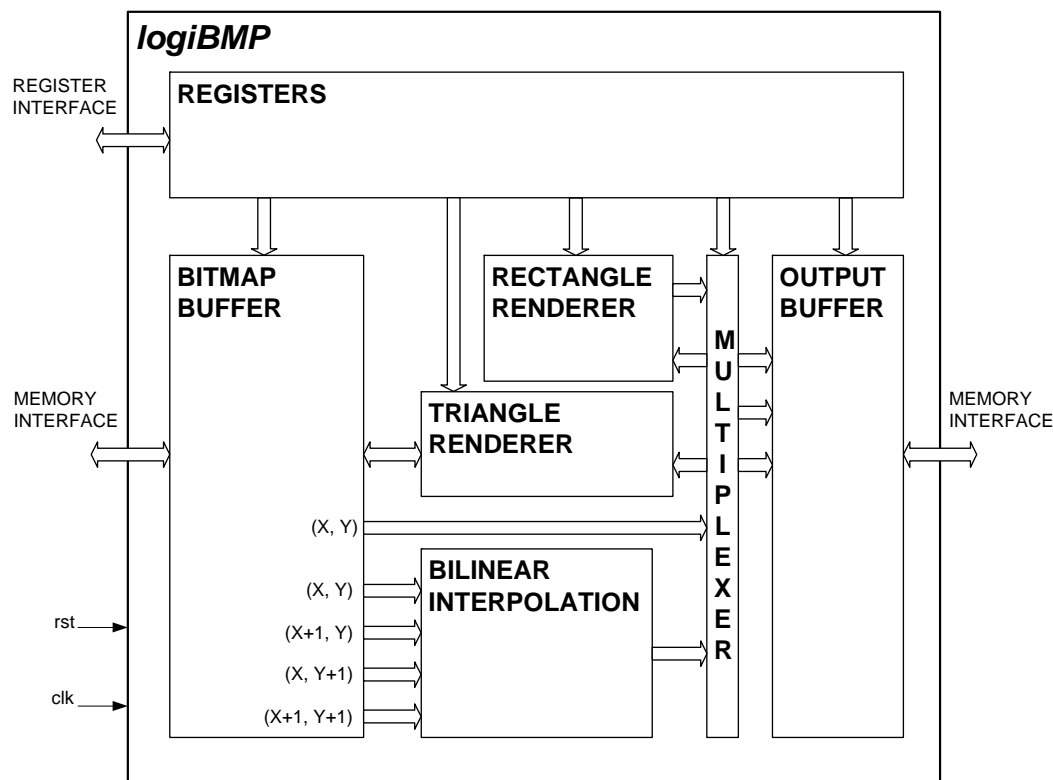


Figure 1: logiBMP Architecture

Features (cont):

- Prepared for Xilinx Platform Studio (XPS) and the EDK
- IP core configuration through VHDL parameterization enables features vs. slice consumption tunings
- Simple Plug'n'Play with other Xylon logicBRICKS™ IP cores, such as:
 - logiMEM Flexible Memory Controller
 - logiBITBLT Bit Block Transfer 2D Graphics Accelerator
 - logiCVC-ML Compact Multi Layer Video Controller

Applications

- All kinds of GUI based embedded systems
- Car infotainment
- Auto PCs, Hand-held PCs
- Personal Digital Assistants
- Set Top Boxes, Video Phones
- Electronic Gadgets, etc.

General Description

The logiBMP Bitmap 2.5D Graphics Accelerator is an IP core from Xylon logicBRICKS™ IP library, optimized for Xilinx FPGAs and designed to speed up graphics operations with bitmaps. The logiBMP Bitmap 2.5 Graphics Accelerator core significantly speeds up GUI rendering. It supports very complex bitmap operations like texture rendering, picture filtering, up and down scaling, and bitmap rotation. In combination with the logiBITBLT Bit Block Transfer 2D graphics accelerator it supports smooth transitions and animations, and adds a real “wow” effect to the GUI.

The logiBMP performs operations in one memory region (source block of data) and stores results to another memory region (destination block of data). It transforms and copies bitmaps from or to the video memory.

Resulting (transformed) bitmap is created as a combination of the content of source memory region and parameters stored in logiBMP registers.

The logiBMP is designed for integration with the logiCVC-ML Compact Multi Layer Video Controller, the logiBITBLT Bit Block 2D graphics accelerator, and the logiMEM (Flexible SDR/DDR/DDR2/DDR3 memory controller). Please visit <http://www.logicbricks.com/Products/IP-Cores.aspx> to learn more about these IP cores.

It can be easily integrated with other logicBRICKS™ IP cores, as well as with third-party designed IP cores.

Functional Description

The logiBMP graphics accelerator is partitioned into modules as shown in Figure 1: registers, bitmap buffer, triangle renderer, rectangle renderer, bilinear interpolation, and output buffer.

Registers

The register interface allows users to make real-time changes of the logiBMP parameters by software. The registers can be configured as the CoreConnect OPB or PLB compatible slave interface.

Bitmap buffer

Bitmap buffer fetches source bitmap (texture) from an external memory. Implemented bitmap cache increases the memory bandwidth utilization. Fast memory interface can be configured as the CoreConnect PLB or Xylon XMB compatible master memory interface.

Triangle renderer

The triangle renderer block renders triangle with a source bitmap. The triangle renderer calculates coordinates of pixels within the defined triangle, coordinates of corresponding texels (pixel in source bitmap – texture) for point sampling, and coordinates of neighboring texels for bilinear interpolation.

Rectangle renderer

Solid fill - rectangle rendering operations are performed by the rectangle renderer. This block fills rectangles with the defined color, and its functions enable very useful graphics operations as, for an example, the clear screen function.

Bilinear interpolation

The bilinear interpolation block performs linear interpolation in both directions, first in the horizontal direction and then in the vertical direction. The block calculates resulting pixels from four neighboring pixels sourced by the bitmap buffer, and fraction parts of pixel coordinates sourced by the triangle renderer.

Output buffer

The output buffer stores processed pixels to the video memory. An implemented FIFO optimizes and increases the utilization of available memory bandwidth. The fast memory interface can be configured as the CoreConnect PLB or Xylon XMB compatible master memory interface.

Core Modifications

The core is supplied in an encrypted VHDL format with simulation vectors. Many logiBMP configuration parameters are selectable prior to VHDL synthesis, and the following table presents some illustrative examples:

Table 2: logiBMP VHDL configuration parameters

Parameter	Description
C_READABLE_REGS	Readable registers: 0 – disable, 1 - enable
C_VIDEO_STRIDE_WIDTH	Video memory row stride: 9 – 512 pixels, 10 – 1024 pixels, 11 – 2048 pixels
C_USE_VIDEO_STRIDE_REG	Set OUTSTRIDE_REG register to define video memory row stride: 0 – disable, 1 – enable
C_XY_WIDTH	Maximal width of (x, y) coordinates
C_UV_WIDTH	Maximal width of (u, v) coordinates
C_USE_SOLID_FILL	Use solid fill operation (rectangle rendering): 0 – disable, 1 – enable
C_CACHE_LINE_SIZE	Line size of texture cache: 3 – 2 pixels, 4 – 4 pixels, 5 – 8 pixels, 6 – 16 pixels
C_CACHE_DEPTH	Depth of texture cache: 11 – 2kB, 12 – 4kB, 13 – 8kB, 14 – 16kB, 15 – 32kB, 16 – 64kB
C_USE_2_5D_MODE	Use perspective correct rendering option: 0 – disable, 1 – enable

There may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiBMP core or to supplement some of your specific functions, you can allow us to tailor the logiBMP to your requirements.

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
rst	Input	Global synchronous set/reset
clk	Input	Global clock input (memory clock) – the same clock is used for memory interface (XMB memory interface clock or PLB master bus clock)
Memory Interface		
PLBV46 Master Interface	Bus	Refer to Xilinx-IBM CoreConnect specification
XMB Interface	Bus	Xylon Memory Bus – refer to logiMEM user's manual
Register Interface		
PLBV46 Slave Interface	Bus	Refer to Xilinx-IBM CoreConnect specification
OPB Slave Interface	Bus	Refer to Xilinx-IBM CoreConnect specification

Verification Methods

The logiBMP is fully supported by the Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiBMP implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon logicBRICKS™ IP cores can be evaluated on Xylon's logiCRAFT6 and logiTAP development platforms, which are designed especially for developers working in the fields of multimedia and infotainment. The platforms demonstrate modularity on all levels: software, board, FPGA, and IP cores. The logiCRAFT6 and the logiTAP platforms make excellent development tools particularly appropriate for the development of embedded systems with strong graphics capabilities.

To learn more about the logiCRAFT6 Multimedia Evaluation/Development Platform, please visit:

URL: <http://www.logicbricks.com/Products/logiCRAFT6.aspx>

To learn more about the logiTAP Platform for Embedded GUI System Developments, please visit:

URL: <http://www.logicbricks.com/Products/logiTAP.aspx>

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com

URL: www.logicbricks.com

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.06	03.01.2011.	Initial Xylon release – new doc template