

Xylon d.o.o.

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Features

- Supports all Xilinx FPGA families
- Supports LCD and CRT displays (easily tailored for special display types)
- 64x1 to 2048x2048 display resolutions
- Higher resolutions support available on request
- Supports up to 5 layers; the last one configurable as a background color
- Configurable layers' size, position and offset
- Alpha blending and Color keyed transparency
- Pixel, Layer, or Color lookup table (CLUT) alpha blending mode can be set for each layer independently
- Packed pixel layer memory organization – pixel color depth 8bpp, 8bpp using Color Look up Table, 16bpp Hicolor RGB 5-6-5 and Truecolor 24bpp
- Configurable PLBv4.6, XMB or AXI4 memory interface data width (32, 64 or 128)
- Support for multiple output formats:
 - Parallel display data bus: 12x2-bit, 15-bit, 16-bit, 18-bit or 24-bit
 - Digital Video ITU-656: PAL and NTSC
 - LVDS output format: 3 or 4 data pairs plus clock
 - Camera link output format: 4 data pairs plus clock
 - DVI output format

Core Facts	
Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design ucf
Verification	Reference design simulation
Reference Designs & Application Notes	XPS reference design Application note
Additional Items	logiCRAFT6 evaluation board logiTAP evaluation platform logiCRAFT-CC evaluation platform SW drivers
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)			LCs	Slices ¹ (FFs/ LUTs)	IOB ²	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
	mclk	vcclk	rclk									
Spartan®-3E (XC3S1200E-5)	361	116	112	968	430 (396/446)	32	N/A	2	0	0	N/A	ISE® 12.4
Spartan®-6 (XC6SLX25-3)	575	206	173	1952	305 (404/605)	32	0	2	0	0	0	ISE® 12.4
Virtex®-5 (XC5VLX50-3)	545	351	334	1620	253 (394/401)	32	0	2	0	0	0	ISE® 12.4
Virtex®-6 (XC6VLX75T-3)	605	434	402	1453	227 (391/386)	32	0	2	0	0	0	ISE® 12.4

Notes:

- 1) Assuming the following configuration: RGB888 output, 1x24 bit layer, 32-bit PLB registers interface and memory interface XMB
- 2) Assuming only display control signals are routed off-chip, register and memory interfaces are connected internally

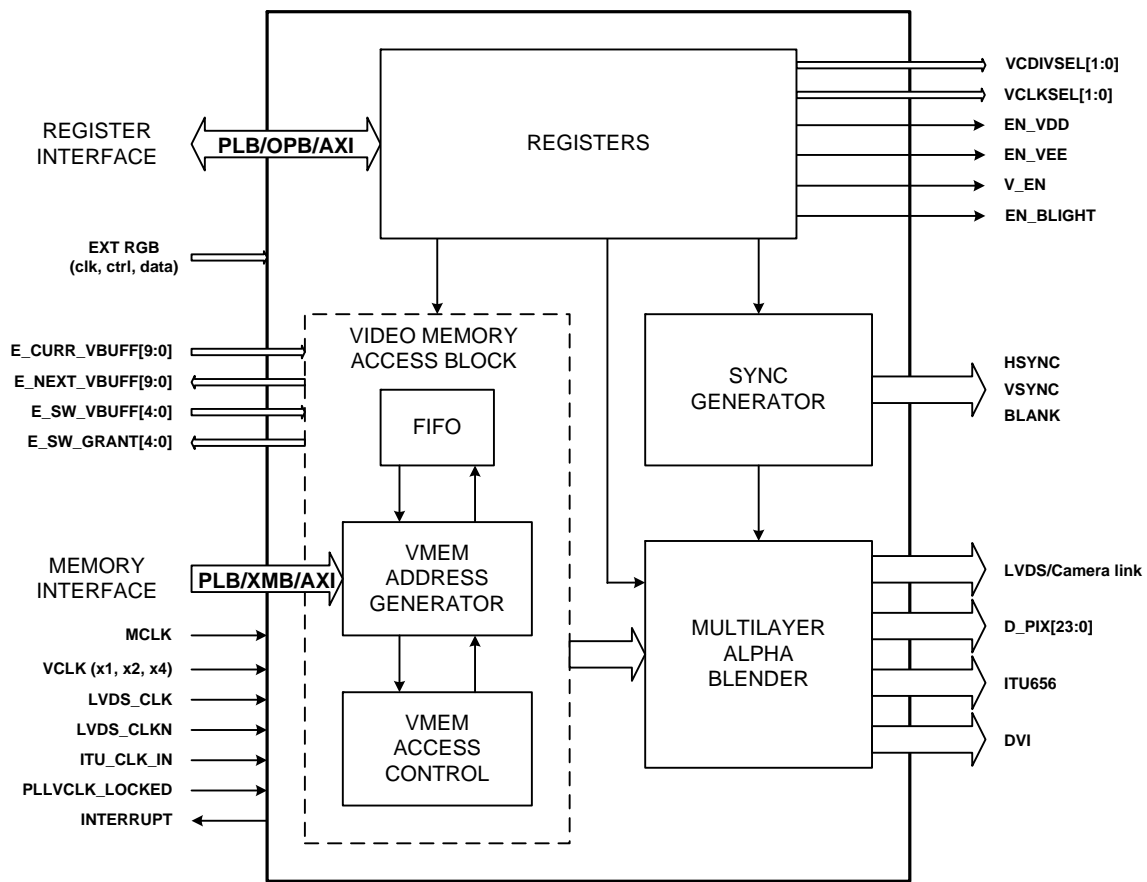


Figure 1: logiCVC-ML Architecture

Features (cont)

- Simple programming of control registers over OPB, PLBv4.6 or AXI4-Lite interface
- Programmable layer memory base address and stride
- HW cursors
- Supports synchronization to external parallel RGB input (data used for one layer)
- Double/triple buffering enables flicker free reproduction
- Display power-on sequencing control signals
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Prepared for Xilinx Platform Studio (XPS) and the EDK
- Simple Plug'n'Play with other Xylon logicBRICKS™ IP cores, such as:
 - logiMEM Flexible Memory Controller
 - logiBITBLT Bit Block Transfer 2D Graphics Accelerator
 - logiBMP Bitmap 2.5D Graphics Accelerator
 - logiWIN Versatile Video Controller

Applications

- Car Infotainment and Telematics
- AutoPCs, Hand-held PCs
- Personal Digital Assistants
- SetTop Boxes, Video Phones
- Electronic Gadgets, etc.

General Description

The logiCVC-ML - Compact Multilayer Video Controller is a graphic video controller optimized for Xilinx FPGAs. It controls TFT flat panel displays, DVI monitors and, by means of external video converters, S-Video, Composite Video devices and CRT displays (i.e. VGA monitors) and CVBS displays. A scaled-down logiCVC is available on request for non-TFT flat panel displays (TNM, STNM, etc.)

Multilayer support provides on screen display functions: alpha blending, color keyed transparency among layers, hardware cursors and fast scrolling and pan functions. All these features are supported in hardware and therefore require only low CPU processing power.

The interface to the frame buffer, or the video memory, is designed for SDRAM (SDR, DDR, DDR2) or SRAM implementation. For easier system integration, logiCVC-ML uses Xilinx (IBM) CoreConnect PLBv46, OPB and AXI (AMBA) buses. The logiCVC-ML requires relatively low memory bandwidth and can be efficiently implemented in low-cost systems featuring Unified Memory Architecture (UMA).

Functional Description

The logiCVC-ML internal structure is shown on the block diagram on Figure 1.

The logiCVC-ML's functional blocks are: Video Memory Access Block, Video Address Generator, FIFOs, Sync Generator, Multilayer Alpha Blender, Registers.

Video Memory Access Block

The Video Memory Access Block consists of 3 sub modules: Video Memory Access Control, Video Memory Address Generator and FIFOs. The Video Memory Access Block fetches video data from the video memory over PLBv4.6, XMB (Xylon Memory bus) or AXI4 to the local FIFOs. The Video Address Generator calculates video memory pointers for each layer. The Video Memory Access Block ensures that each FIFO is filled with the required amount of pixels and it performs arbitration between memory requests of each layer.

There is one FIFO per layer used for temporary storage of pixels. The FIFOs optimize the usage of video memory bandwidth and resynchronize incoming data to the display clock.

Sync Generator

The Sync Generator generates video synchronization signals. The duration of sync signals and their relative position to the display data (i.e., visible picture on the screen) can be adjusted through the set of logiCVC-ML registers. Additionally, external RGB input stream can be used for synchronization and sync generation.

Multilayer Alpha Blender

The Multilayer Alpha blender block consists of 5 equal configurable layer blocks. The outputs of the layer blocks are mixed according to alpha/transparent factors and layer priority. The Blender supports layer, pixel and color alpha blending methods.

Registers

All logiCVC-ML registers are instantiated in this block. The CPU has access to all these registers through an OPB (On-chip Peripheral Bus), PLBv4.6 or AXI4-Lite bus.

Core Modifications

The core is supplied in an encrypted VHDL format, with simulation vectors. The following logiCVC-ML configuration parameters are selectable prior to VHDL synthesis:

Table 2: logiCVC VHDL configuration parameters

Parameter	Description
C_DISPLAY_INTERFACE	Video output type: RGB, ITU656, LVDS, camera link, DVI
C_PIXEL_DATA_WIDTH	RGB data output width
C_USE_SIZE_POSITION	Layer size, position and offset functionality implementation on/off
C_NUM_OF_LAYERS	Number of layers (up to 5)
C_LAYER_X_DATA_WIDTH	Layer X data width
C_LAYER_X_ALPHA_MODE	Layer X alpha blending mode
C_LAYER_X_OFFSET	Layer X offset
C_BUFFER_X_OFFSET	Layer X buffer offset
C_USE_BACKGROUND	Last layer configuration as background on/off
C_USE_SERIALIZED_BLENDER	Only one set of multipliers on higher frequency for alpha blending implementation on/off
C_USE_MULTIPLIER	Defines type of multipliers
C_USE_XTREME_DSP	DSP resources implementation on/off
C_USE_E_RGB_INPUT	Syncronize logiCVC to external RGB input and use data as one layer on/off
C_E_DATA_WIDTH	Extern RGB layer data width

The logiCVC-ML has been constructed with regard to adaptability to various display types and has been tested on several popular displays. However, there may be instances where source code modification would be necessary. Therefore, if you wish to reach the optimal use of the logiCVC-ML core or to supplement some of your specific functions, you can order the source code or allow us to tailor the logiCVC-ML to your requirements. The logiCVC-ML source code (VHDL sources) is available at additional cost from Xylon.

Core I/O Signals

The core signal I/Os have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/Os are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
RST	Input	Global synchronous set/reset
Memory Interface		
PLBV46 Master Interface	Bus	Refer to Xilinx-IBM Core connect specification
XMB Interface	Bus	Xylon Memory Bus. Refer logiMEM specification
AXI4 Master Interface	Bus	Refer to AMBA AXI version 4 specification from ARM
Register Interface		
PLBV46 Slave Interface	Bus	Refer to Xilinx-IBM Core connect specification
OPB Slave Interface	Bus	Refer to Xilinx-IBM Core connect specification
AXI4-Lite Interface	Bus	Refer to AMBA AXI version 4 specification from ARM
Display Control Signals		
HSYNC	Output	Horizontal sync

Signal	Signal Direction	Description
VSYNC	Output	Vertical sync
PIX_CLK	Output	Pixel clock
PIX_CLKN	Output	Pixel clock inverted
BLANK	Output	Blank/display enable at TFT
D_PIX[n : 0]	Output	Video pixel data bus
LVDS_DATA_OUT_P[3:0]	Output	LVDS pixel data, positive
LVDS_DATA_OUT_N[3:0]	Output	LVDS pixel data, negative
LVDS_CLK_OUT_P	Output	LVDS clock, positive
LVDS_CLK_OUT_N	Output	LVDS clock, negative
ITU656_CLK	Output	ITU656 clock
ITU656_DATA[7:0]	Output	ITU656 data
DVI_DATA_OUT_P[2:0]	Output	DVI pixel data, positive
DVI_DATA_OUT_N[2:0]	Output	DVI pixel data, negative
DVI_CLK_OUT_P	Output	DVI clock, positive
DVI_CLK_OUT_N	Output	DVI clock, negative
Auxiliary Signals		
VCLK	Input	Video clock input
VCLK2	Input	Video clock input x2 (used for serialized blender or 12bit parallel multiplexed output interface)
VCLK4	Input	Video clock input x4 (used for serialized blender, if selected)
PLLCLK_LOCKED	Input	Indication of stable VCLK generated by PLL.
ITU_CLK_IN	Input	ITU656 clock input (27 MHz and synchronous to VCLK)
LVDS_CLK	Input	LVDS clock
LVDS_CLKN	Input	LVDS clock inverted
E_VCLK	Input	External VCLK (used when external RGB input is used)
E_VSYNC	Input	External VSYNC (used when external RGB input is used)
E_HSYNC	Input	External HSYNC (used when external RGB input is used)
E_BLANK	Input	External BLANK (used when external RGB input is used)
E_DATA[n : 0]	Input	External RGB data (used when external RGB input is used)
E_VIDEO_PRESENT	Input	External video present (used when external RGB input is used)
E_CURR_VBUFF[9:0]	Input	Current external stream video memory buffer (two bits per layer)
E_NEXT_VBUFF[9:0]	Output	Next external stream video memory buffer to write to (two bits per source)
E_SW_VBUFF[4:0]	Input	External switch logiCVC-ML video memory buffers (one bit per layer)
E_SW_GRANT[4:0]	Output	External switch grant (one bit per source, handshaking signal for E_SW_VBUFF)
VCDIVSEL[1:0]	Output	Video clock divider select
VCLKSEL[2:0]	Output	Video clock select
INTERRUPT	Output	CVC Interrupt signal, level sensitive, high active
EN_VDD	Output	Enable Vdd power supply
EN_BLIGHT	Output	Enable backlight power supply
V_EN	Output	Enable display control/data signals
EN_VEE	Output	Enable Vee power supply

Verification Methods

The logiCVC-ML is fully supported by the Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiCVC-ML implementation does not require any particular skills beyond general Xilinx tools knowledge. The encrypted IP is shipped with reference design and compiled simulation libraries for ModelSim.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon logicBRICKS™ IP cores can be evaluated on logiCRAFT6 Xylon development platform, which is designed especially for developers working in the fields of multimedia and infotainment. This platform demonstrates modularity on all levels: software, board, FPGA, and IP cores. The platform makes excellent development tool particularly appropriate for the development of embedded systems with strong graphics capabilities.

To learn more about the Xylon development platforms, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com

Ordering Information

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
1.06.	09.04.2010.	New doc template
2.00.	15.09.2010.	AXI Interface update
2.01.	14.03.2011.	DVI output interface support