

Xylon d.o.o.

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Features

- Xilinx® FPGA compatible IP core
- Supports perspective transformations of 2D quadrilaterals
- Programmable homographic transformation matrix enables:
 - cropping
 - resizing
 - rotating
 - translating
 - arbitrary combination of above operations
- Supports correction of fish eye lens distortions
- Suitable for extreme wide-angle lenses (fish-eye) with Field Of View (FOV) >180°
- Calibration software enables lens and automotive Surround View DA calibration with preview option
- Configurable number of video inputs (cameras)
- Configurable number of video outputs
- Input and output resolutions, and frame per second (fps) rates depend on overall system's architecture
- Supports 2048x2048 and higher input and output resolutions

Core Facts	
Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference design ucf
Verification	Reference design simulation
Reference Designs & Application Notes	XPS reference design
Additional Items	logiVIEW Calibration Software and SW drivers logiVIEW-SVK Development Platform and Toolset for Automotive Four-Camera Surround View DA
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)	LCs	Slices ¹ (FFs/ LUTs)	IOB ²	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
	mclk									
Spartan®-3A (XC3SD1800A-5)	107	12618	5608 (5193/6460)	0	0	22	22	0	N/A	ISE® 12.4
Spartan®-6 (XC6SLX25-2)	165	18131	2833 (5406/4699)	0	0	22	22	0	N/A	ISE® 12.4
Virtex®-5 (XC5VLX30-3)	235	21440	3350 (4968/4934)	0	0	12	22	0	N/A	ISE® 12.4
Virtex®-6 (XC6VLX75T-3)	290	15827	2473 (5034/4278)	0	0	22	22	2	N/A	ISE® 12.4

Notes:

- 1) Assuming the Automotive Surround View Driver Assistance (DA) system's configuration: 4 input cameras, 4 output images, 32-bit PLB registers, 64-bit memory interface, lens correction and perspective transformation
- 2) Assuming register and memory interfaces are connected internally
- 3) The slice count is reduced for approximately 10% with disabled registers

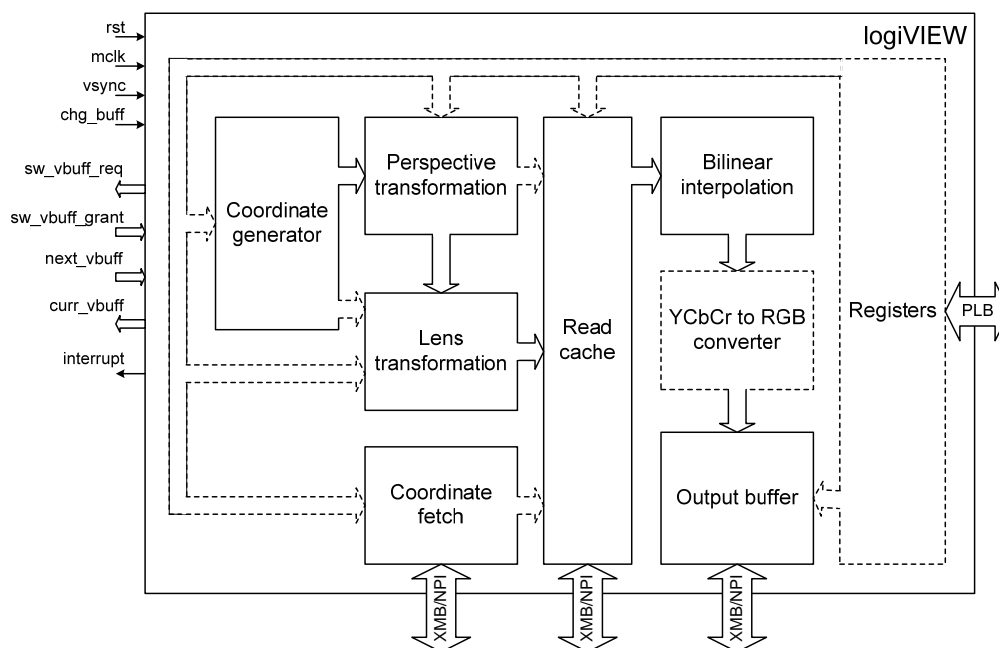


Figure 1: logiVIEW Architecture

Features (cont)

- Supports 30 fps and higher frame rates
- Supports input/output color space combinations: RGB/ RGB, YCbCr(4:2:2)/ RGB and YCbCr(4:2:2)/YCbCr(4:2:2)
- Optionally one output image can be processed by the MLUT (Memory Look Up Table) with an arbitrary transformation function
- Double buffering of video inputs and triple buffering of video outputs prevent video flickering
- CoreConnect™ PLB interface allows for an easy interfacing to:
 - on-chip Xilinx MicroBlaze™ microprocessor
 - on-chip PowerPC® microprocessor
 - external microprocessors through PLB compatible bus bridges
- Configurable video memory interface type:
 - XMB (Xylon Memory Bus)
 - Xilinx MPMC (Multi Port Memory Controller)
- Xilinx Platform Studio (XPS) reference design (Four-Camera System for Surround View DA) with the demo software application
- Parametrical VHDL design that allows tuning of features set and consumption of FPGA resources
- Simple Plug'n'Play with other Xylon logicBRICKS™ IP cores, such as the:
 - logiMEM SDR/DDR SDRAM Memory Controller
 - logiBAYER Color Camera Sensor Bayer Decoder
 - logiWIN Versatile Video Input
 - logiCVC-ML Compact Multilayer Video Controller
 - logiBITBLT Bit Block Transfer 2D Graphics Accelerator

Applications

- Automotive Driver Assistance Systems: Surround View (Bird's Eye View), Rear-View Camera, HUD, others
- Industrial systems: Surveillance Systems, Industrial Pipe Inspection equipment and others
- Medical Endoscopy and similar equipment
- Defense equipment, etc.

General Description

The logiVIEW is Xylon's logicBRICKS™ IP core optimized for Xilinx FPGAs and designed to process still images or video streams in a real-time. The logiVIEW IP core removes fish eye distortions caused by extreme wide-angle field of view (FOV) lenses, makes perspective corrections to the captured video and stitches multiple corrected video inputs or still images in a resulting single image for the LCD display.

The logiVIEW can be used in automotive Driver Assistance (DA) applications, such as the Four-Camera System for Surround View DA (Figure 4), Heads-Up Displays (HUD) or rear-view camera (backup aid) systems. Due to its high versatility and configurability, it can be used in other single or multi-camera applications, such as a medical endoscopy, surveillance systems, defense equipment, etc.

The image compensation for fish eye distortions caused by wide-angle FOV lenses rectilinearly projects the camera captured images on the flat 2D surface suited for the LCD display. Perspective transformations calculated by a programmable homographic transformation matrix enable scaling, rotation, cropping, translation, as well as simultaneous combinations of all of these transformations. The Figure 2 shows several example outputs.

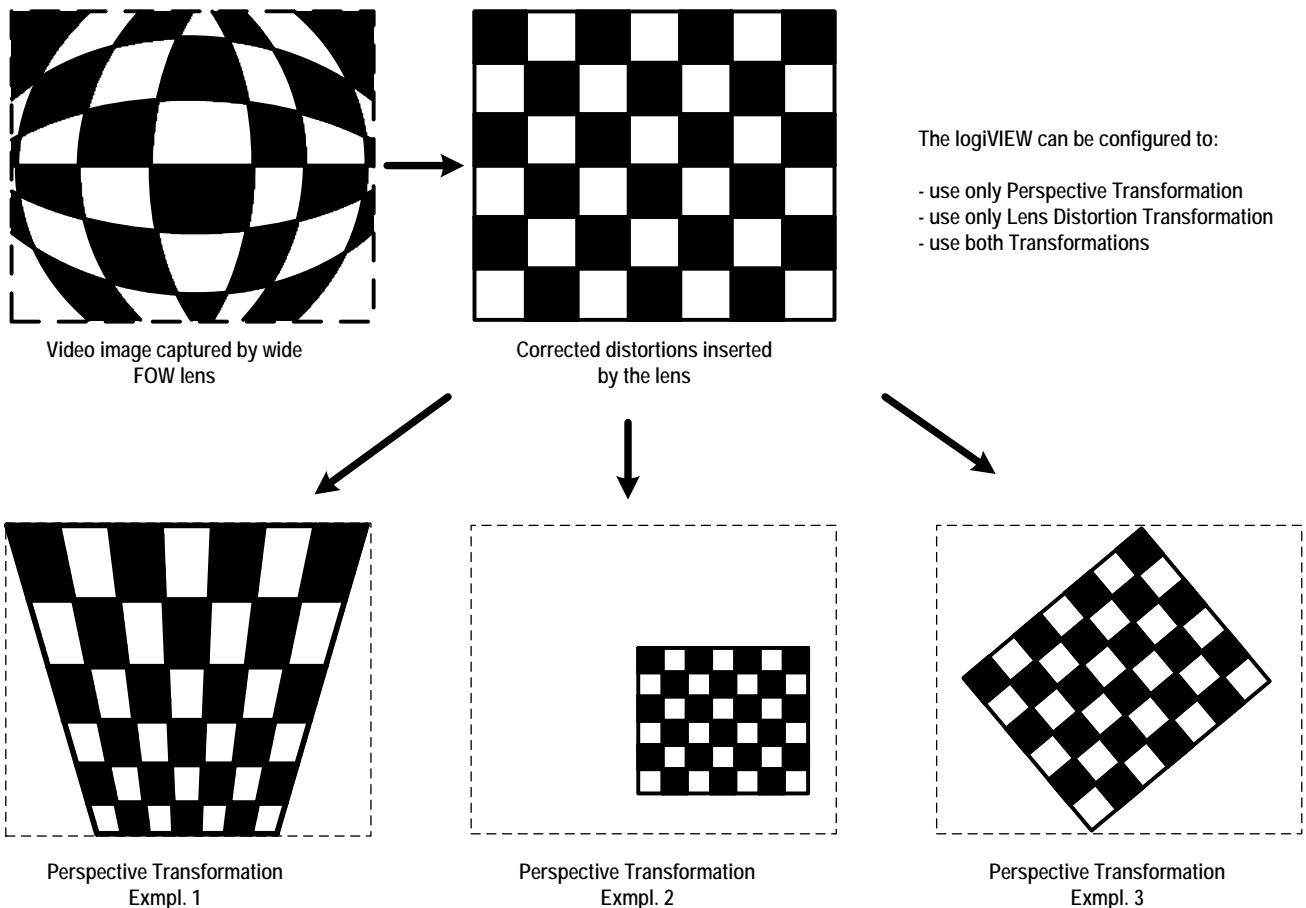


Figure 2: logiVIEW Processing Flow with Perspective Transformation Examples

The logiVIEW is a highly configurable IP core and can be used within Xilinx Platform Studio and the EDK implementation tools. Xilinx implementation tools enable easy tuning of the logiVIEW's consumption of FPGA resources and the features set setup through an easy-to-use GUI interface. Table 2 shows configuration parameters that can be setup prior to the core's synthesis time. IP configurations which utilize only the

perspective, or only the lens transformation, are good examples of balancing between the required features set and used FPGA resources.

The logiVIEW can handle an arbitrary number of video inputs and video outputs as long as the system architecture allows it. The available memory bandwidth, frame rates of input video cameras, and similar system parameters, determine the number of supportable video inputs and outputs by a single logiVIEW IP core.

For example, the YCbCr video format requires lower memory bandwidth than the RGB video format, and the logiVIEW IP core configured to use the YCbCr can support more video channels and higher video resolutions with the same memory subsystem (SoC bus and memory controller IP core) and the memory connected to the FPGA. Video format can be setup through IP core's configuration GUI interface.

The logiVIEW-SVK Development Platform and Toolset for Surround View DA implements the logiVIEW IP core configured to support 4 camera systems, megapixel resolutions and 30 fps.

The logiVIEW has a programmable registers field accessible through the standard CoreConnect PLB bus. The PLB bus enables easy interconnections with various processors, such as the Xilinx MicroBlaze and the PowerPC. Video memory interface can be selected to support Xilinx MPMC memory controller or a highly optimized Xylon XMB bus.

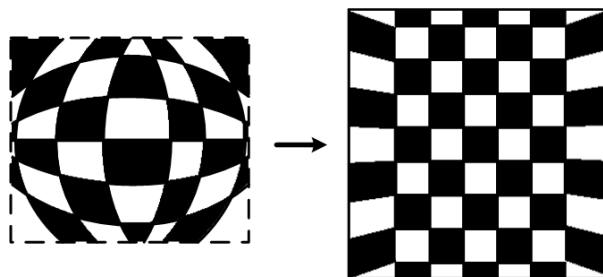


Figure 3: Example MLUT Transformation

The logiVIEW IP core can be configured to use an optional Memory Look Up Table (MLUT) block at one video output. The MLUT can be programmed with an arbitrary transformation function which executes different transformations on input video picture's parts, for example an gradual compensation of fisheye lens distortions at picture's edges and a full removal of all distortions in the picture's center (Figure 3).

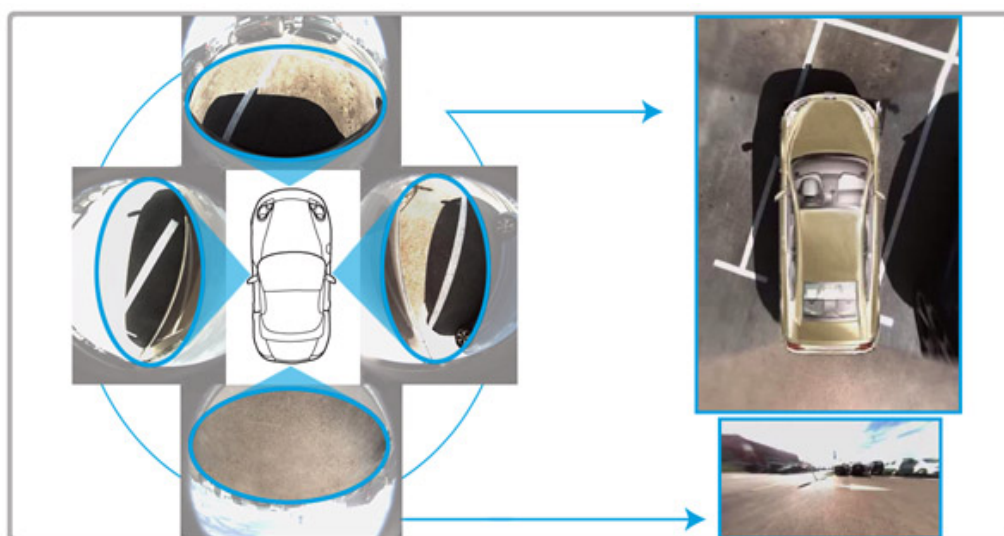


Figure 4: logiVIEW Application Example – Xylon's Four-Camera Surround View DA Demo System

The Figure 4 provides an illustrative example of the logiVIEW capabilities. Snapshot comes from Xylon's Four-Camera Surround View DA Demo System, which is mounted on the test vehicle. The Surround View DA provides an unmatched awareness of the situation by enabling the driver to see 360-degrees around the vehicle on the LCD instrument cluster or the Central information Display (CID). The surroundings can be seen top-down from a bird's eye view perspective, which eliminates all blind spots during critical and precise maneuvers in crowded spaces.

The Surround View DA system uses 4 cameras, furnished by extreme wide-angle fish eye lenses, which cover separated zones around the vehicle. The logiVIEW must remove the lens distortions and correct the perspectives to four high-resolution input video streams, and stitch the corrected video images in a single display of vehicle's surroundings. Correct image stitching is very challenging due to overlapping of camera captured scenes caused by the extreme wide-angle FOV lenses.

logiVIEW Calibration Software

Precise matching to a specific wide-angle FOV lens, and the vehicle's model for Surround View DA designs, requires an extensive software support. Xylon provides the two-phase software for the calibration of various camera (lens) parameters and camera positioning on the vehicle. The calibration software outputs C code and text files for the logiVIEW IP core's initialization.

The first phase is the calibration of all of the system's cameras with extreme wide-angle FOV lenses. The camera (lens) calibration requires the capturing of calibration patterns (images provided by Xylon) and the import of lens and camera parameters, such as the FOV angle and the focal length. The provided preview option prevents the improper corrections of lens fish eye distortions.

The second calibration phase sets up the multi-camera Surround View DA system for a specific vehicle. The shapes of different vehicles require different camera installation points. Each of the system's cameras captures the ground from a different perspective which must be transformed into a bird's eye perspective. The perspective must be corrected and, due to the extreme wide-angle FOV lenses, the overlapping camera outputs must be combined (stitched) into the resulting single image of the vehicle's surroundings.

Find more information about the logiVIEW Calibration Software by visiting:

<http://www.logicbricks.com/Solutions/Surround-View-DA-System/Camera-Lens-Vehicle-Calibration-Software.aspx>

Functional Description

The Figure 1 presents the logiVIEW block diagram. The main logiVIEW functional blocks are: Perspective Transformation, Lens Transformation, Read Cache, and logiVIEW Registers.

Perspective Transformation

The Perspective Transformation calculates the desired perspective transformation defined by the programmable homographic matrix. Output coordinates from the Perspective Transformation can be supplied either to the Lens Transformation block or directly to the Read Cache block if the Lens Transformation is not required.

Lens Transformation

The Lens Transformation can be used with the Perspective Transformation or without it. The generated output pixel coordinates match the calibrated lens parameters. The output coordinates are inputs for the Read Cache block.

Read Cache

The Read Cache block uses coordinates from the Lens Transformation or the Perspective Transformation to retrieve pixels from the original (input) image stored in memory. Besides the pixel defined by input coordinates, the Read Cache block retrieves the nearest neighboring pixels and uses caching for efficient memory bandwidth usage.

logiVIEW Registers

The logiVIEW's registers are accessible through the CoreConnect PLB compatible interface. The registers are optional IP parts, which can be replaced by hard-wired values defined by the VHDL package generated from the logiVIEW Calibration Software.

Core Modifications

The logiVIEW IP core is supplied in an encrypted VHDL format compatible with the Xilinx Platform Studio implementation tools. Many logiVIEW configuration parameters are selectable prior to VHDL synthesis, and the following table presents a selection from a list of the available parameters:

Table 2: logiVIEW VHDL configuration parameters

Parameter	Description
C_NUM_OF_CAM	Number of input cameras or input images
C_MAX_NUM_OF_OP	Maximum number of output images. Used for calculations of the required resources. 1 to C_MAX_NUM_OF_OP images can be used at any time.
C_USE_PT	Use the Perspective Transformation block
C_USE_PT_REGS	Use registers for the Perspective Transformation block. Enables on-the-fly changes of the Homographic Matrix. Valid only if the register interface exists.
C_USE_LT	Use the Lens Transformation block
C_USE_LT_REGS	Use registers for the Lens Transformation block. Enables on-the-fly change of Lens correction. Valid only if the register interface exists.
C_USE_LTP_REGS	Use registers for definition of LUT distribution. It should be enabled for systems utilizing very different types of lenses with different FOVs.
C_USE_MULTIPLIER	Optional use of multipliers in the Bilinear Interpolation block. It increases the number of used Xilinx multiplier blocks, but reduces utilization of LUT and FF resources.
C_BUFFERING_IN	Enables input image's buffering to prevent video flickering.
C_USE_MLUT	Use MLUT table for one output image.
C_USE_YCBCR_IN	Use YCbCr (4:2:2) format for texture/input video stream
C_USE_YCBCR_OUT	Use YCbCr (4:2:2) format for output image
C_WRITE_ALPHA_OB	Enables or disables writing of Alpha Blending constant to the output image memory (when enabled, writes 0xff). This option can be controlled by software if the logiVIEW configuration includes the registers field.

The logiVIEW is designed with regard to adaptability to various SoC designs. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiVIEW core or to supplement some of your specific functions, you can allow us to tailor the logiVIEW to your requirements.

Core I/O Signals

The core signals I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signals I/O are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
RST	Input	Global synchronous set/reset
CLK	Input	Memory clock
Memory Interface		
XMB Interface	Bus	Xylon Memory Bus. Refer to Xylon's logiMEM specifications
NPI Interface	Bus	Refer to Xilinx's Multi Port Memory Controller specifications
Register Interface		
PLBV46 Slave Interface	Bus	Refer to Xilinx-IBM CoreConnect specifications
Video Input Signals		
VSYNC	Input	Vertical Sync
Auxiliary Signals		
CHG_BUFF	Out	Double buffering control (low for buffer 0, high for buffer 1)
CURR_VBUFF	Out	Triple buffering: Current video memory buffer
NEXT_VBUFF	Input	Triple buffering: Next video memory buffer to write to
SW_VBUFF_REQ	Out	Triple buffering: Request for buffer switching
SW_VBUFF_GRANT	Input	Triple buffering: Buffer switching granted
INTERRUPT	Out	Interrupt signal, edge sensitive, active high

Verification Methods

The logiVIEW is fully supported by Xilinx Platform Studio and the EDK integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiVIEW implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

The logiVIEW-SVK Development Platform and Toolset enables automotive designers to quickly start their new Surround View DA design. The toolset includes the reference FPGA design with evaluation logicBRICKS IP cores, calibration and application software, and a full documentation. The hardware platform includes the Xilinx Spartan-6 FPGA SP605 Evaluation Kit with Xylon's add-on FMC board supporting camera connections, four 1-megapixel automotive camera imagers with extreme wide-angle FOV lenses.

To learn more about the logiVIEW-SVK Development Platform, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com/Products/logiVIEW-SVK.aspx

To learn more about the logiFMC-FPD-II 4-Channel FPD-Link-II FMC Daughter Card for connection of 4 cameras, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: www.logicbricks.com/Products/logiFMC-FPD-II.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com/Products/logiVIEW.aspx

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
2.00.	04.06.2010.	Preliminary Xylon release – new doc template
2.00.e	03.03.2011.	Changed data in the Table 2. Added description of new MLUT feature and YCrCB/RGB converter.
2.00.f	01.04.2011	The first public version. Added short Calibration Software description.